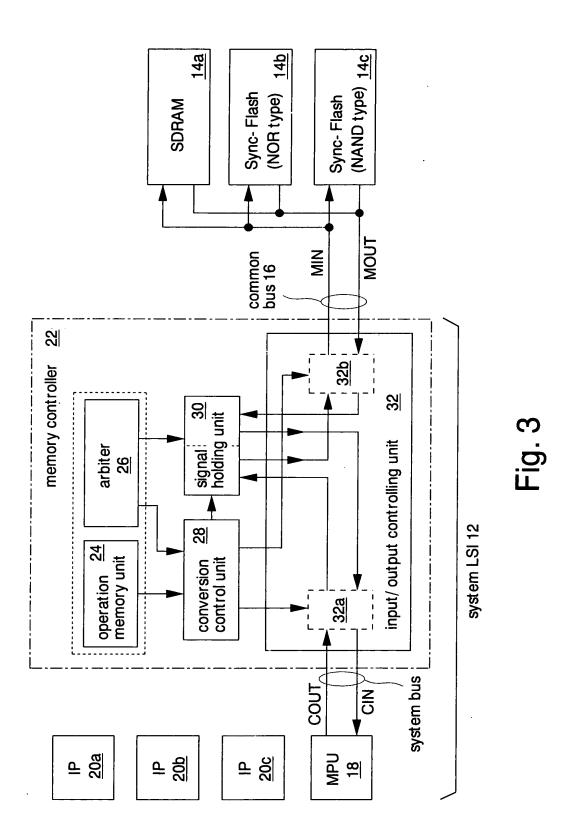


Fig. 2



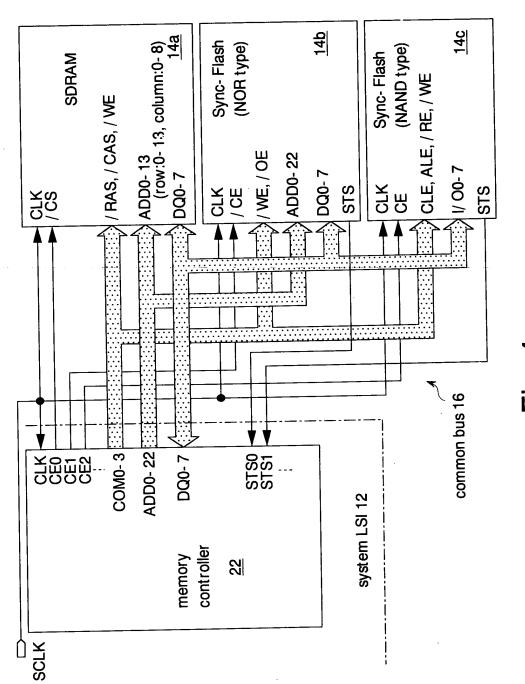


FIG. 4

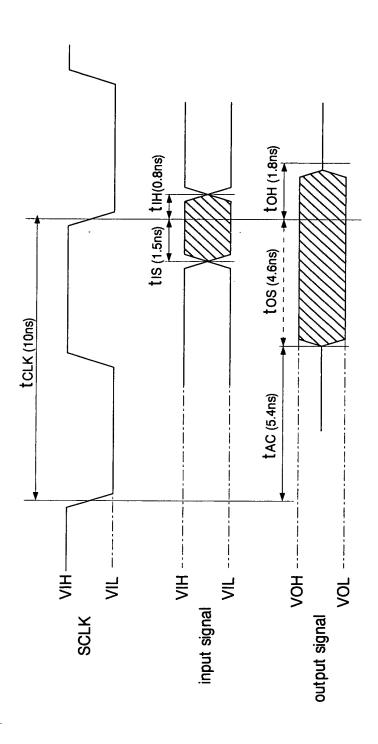


Fig. 5

LVTTL, SSTL	interface of present invention input/ output timing of clock	(sonventional interface) flash memory (sdand) (NAND) wemories
interface level	timing level	operation level (command level)
first class	second class	third class

Fig. 6

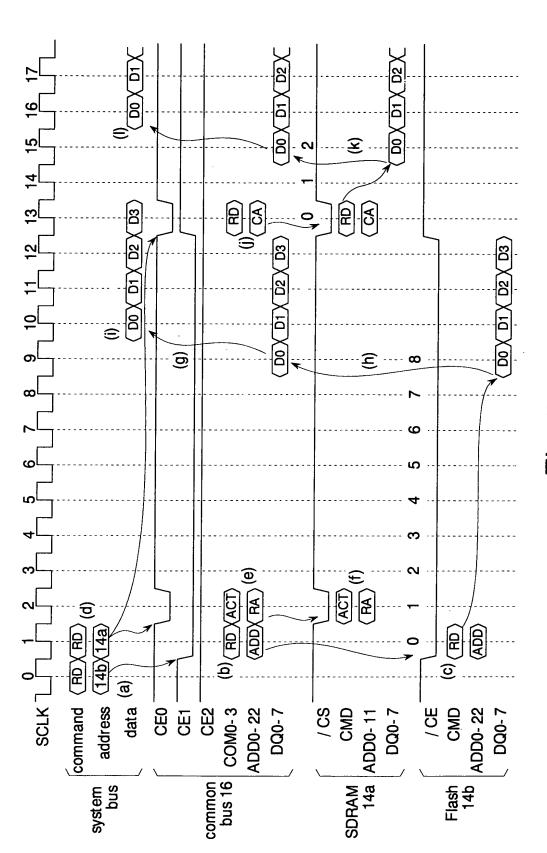
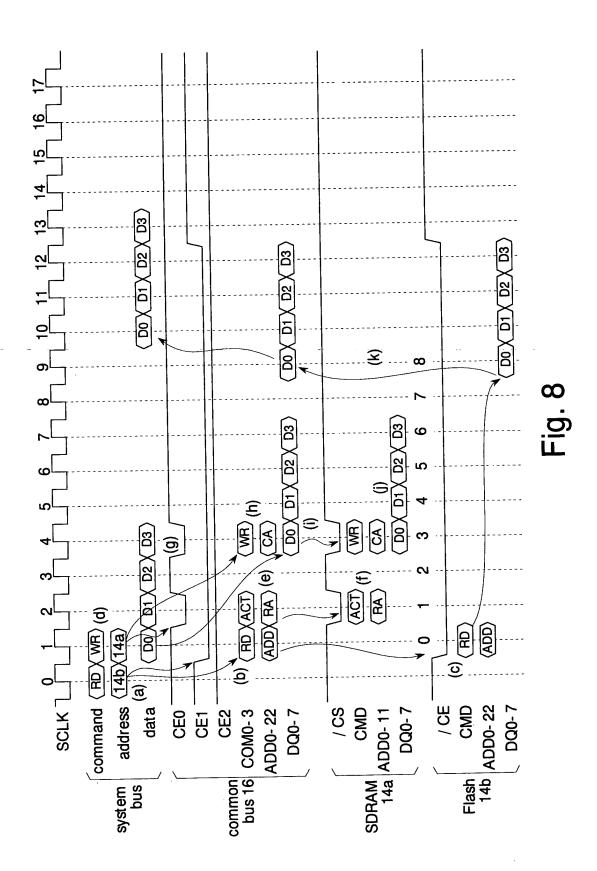


Fig. 7



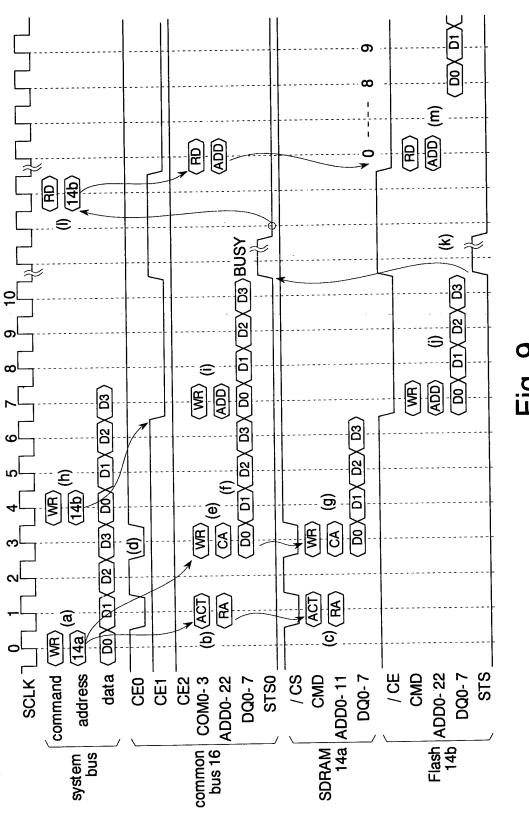


Fig. 9

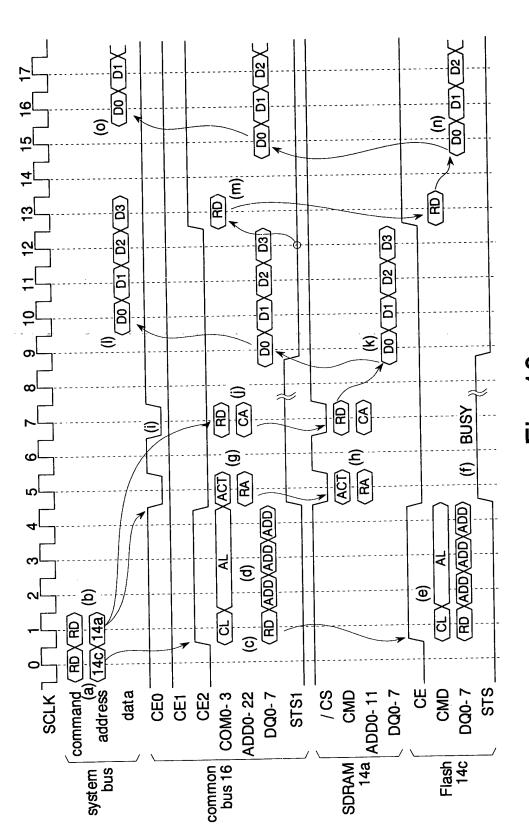


Fig. 10

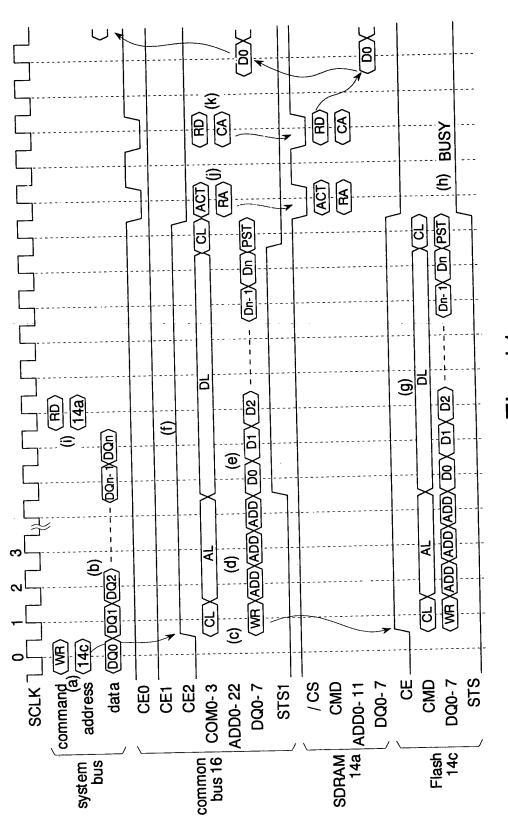


Fig. 11

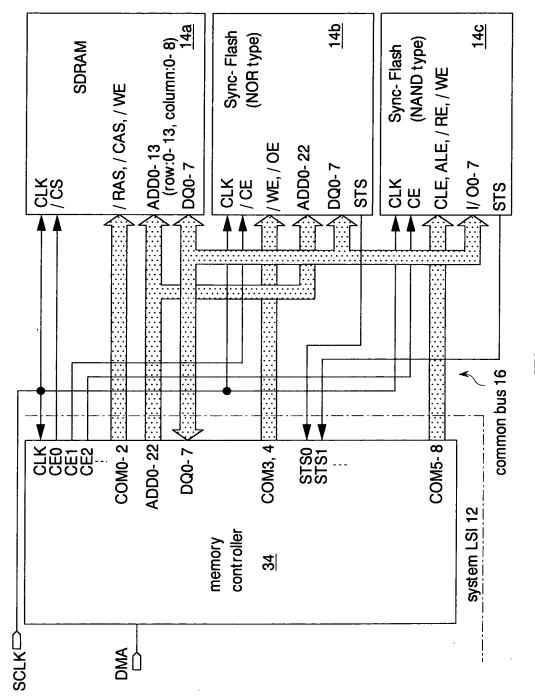
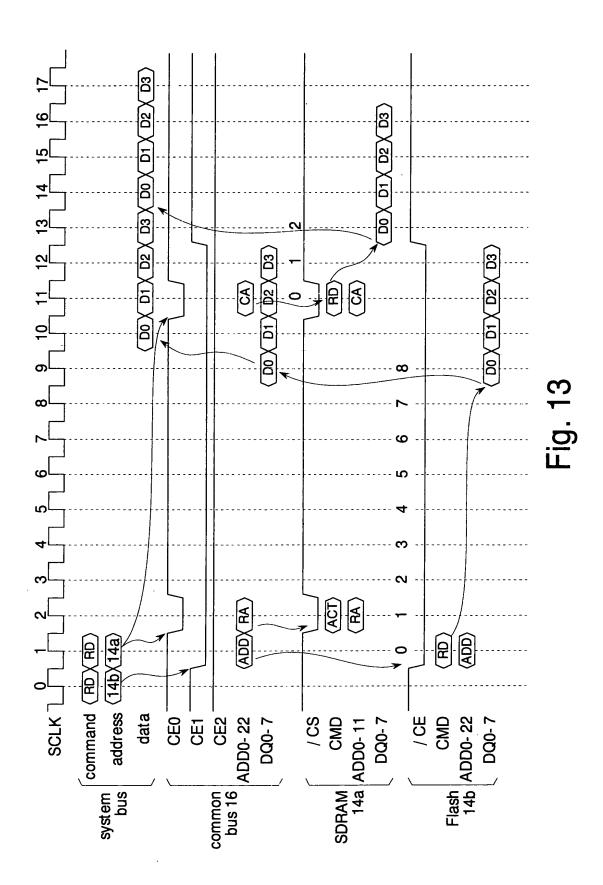


Fig. 12



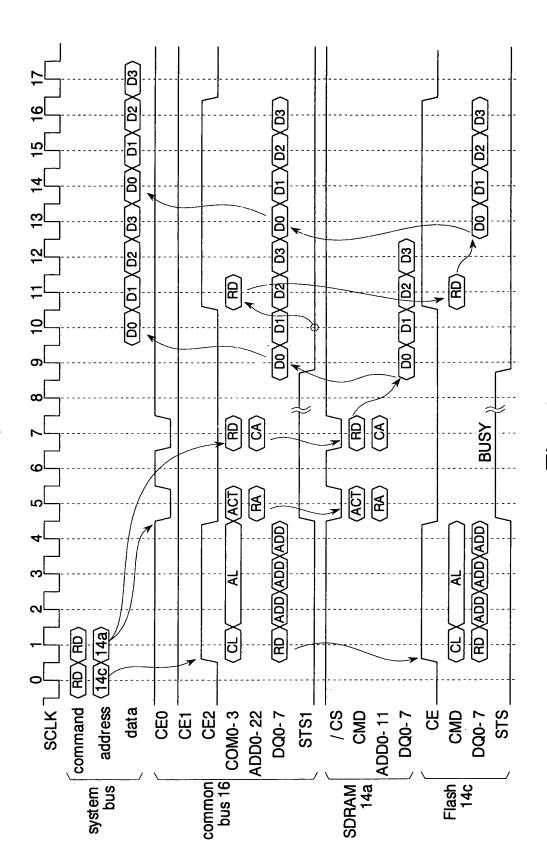
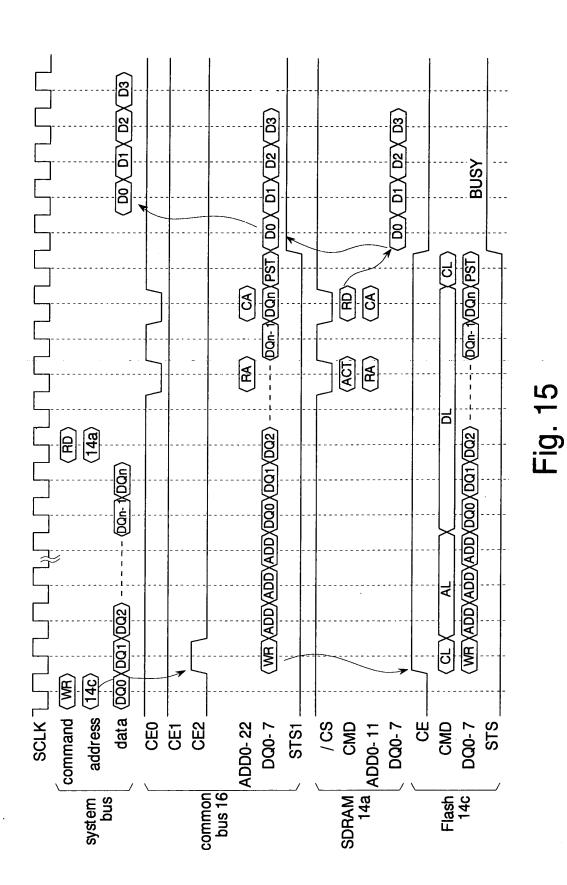
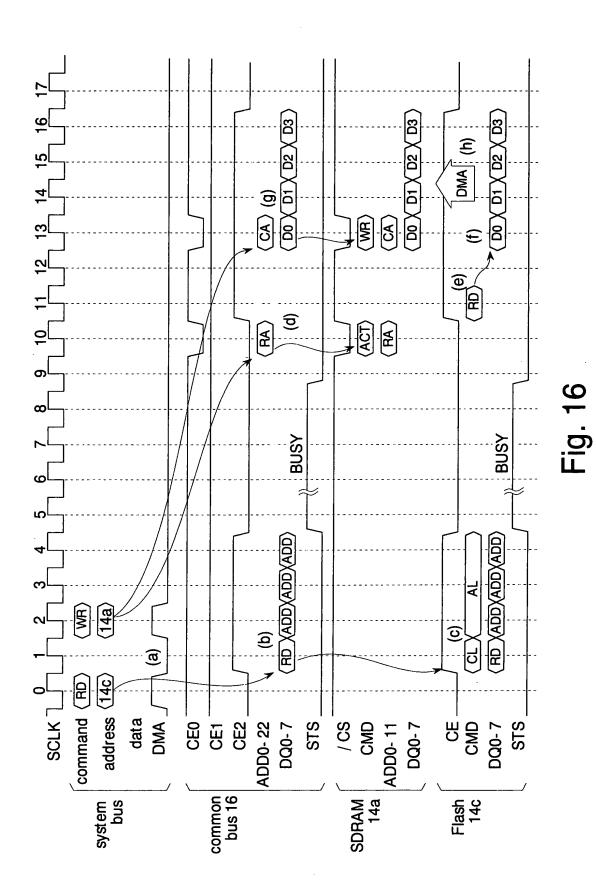
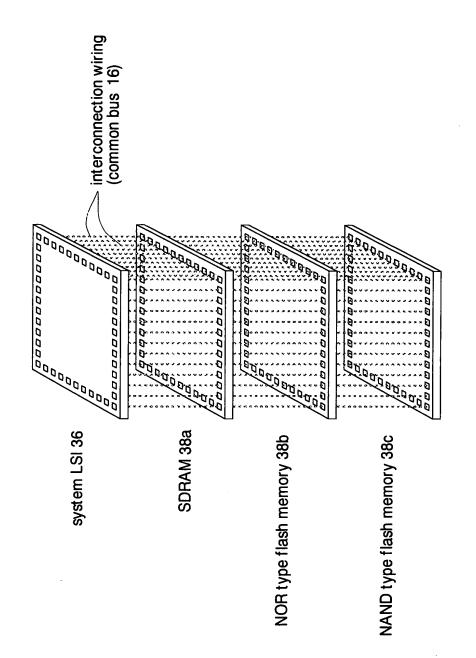


Fig. 14







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